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10/799,783	03/12/2004	Jin-Kyoung Jung	SAM-0529	8323

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,783	JUNG ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-12,14-16,23,25 and 27-44* is/are pending in the application.

4a) Of the above claim(s) *17-22 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12,14-16,23, 25 and 27-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004 and 14 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/2007 has been entered.

2. Claims 1,3,7-12, 14-16, 23, 25, 27-33, 34-44 stand rejected.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, 9, 30-32, 34-35,37, 40, 42 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Rhee et al. (US 6774712).

With respect to claim 1, Figure 4 of Rhee discloses a semiconductor device, comprising: a control signal generating circuit (outputting PDPDEB) for generating a

control signal (PDPDEB) responsive to an input signal (PDPDE) related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (61) coupled to the control signal (PDPDEB), generating circuit for receiving the control signal, the internal voltage generating circuit comprising: a comparing circuit (51) for comparing a reference voltage (output from 41) to an internal voltage (IVC) to generate a driving signal (output at 60) when the control signal is inactivated, wherein the comparing circuit comprises: a comparator (52) connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal; and a switching circuit (58) connected between an external power voltage (+) applied to the comparator when the control signal is activated; a driving signal control circuit (60) for inactivating the driving signal when the control signal is activated; and an internal voltage driving circuit (53) for receiving the external power voltage (+) and generating the internal voltage in response to the driving signal.

With respect to claim 3, figure 4 discloses the device of claim 1, wherein the internal voltage driving circuit (54) includes a PMOS transistor which has a source to

which the external power voltage (+) is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage (IVC) wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to a external power voltage level when the driving signal is inactivated.

With respect to claim 9, an input signal is not a structural component, because a signal has no structure. Furthermore, this operation is inherent in any transistor because an input signal changes the mode between either saturation, active, triode and cutoff modes. The limitation of a plurality of bits is suggested at least in the function of turning on which requires a low bit to high bit operation and encompasses at least two bits. This limitation is also intended use because an input signal can be used in any device.

With respect to claims 30-32, these claims are deemed to be intended use. (Note: any value or number of bits input would correspond to the number of bits processed by the semiconductor because the input and the value of the bits have a causal effect on the semiconductor.) Also an input signal can be used in any device.

With respect to claims 34-35 and 37 are rejected for similar reasons as above.

With respect to claims 40, 42 and 44 the PMOS device or the NMOS device meet the claimed limitation because they are activated when at least a single bit in input. Furthermore these claim limitations are deemed inherent since the claimed structure is fully anticipated by Rhee et al.

With respect to claims 41, 43 and 39 these claim limitations are deemed inherent since the claimed structure is fully anticipated by Rhee et al.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. (US 6774712) in view of Sher.

With respect to claim 7-8, figure 4 of Rhee discloses the device of claim 1 but fails to disclose wherein the control signal generating circuit comprises a fuse to generate the control signal responsive to the input signal. Figure 1 and 18 of Sher teach using a bond pad with a fuse to generate an input signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the bond pad and the fuse in Sher in the control signal generating circuit of Rhee for the purpose of protecting the control signal generating circuit from an high current.

3. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. (US 6774712)in view of Bae et al. (US 6373754).

With respect to claim 2, figure 4 teaches the device of claim 1, wherein the driving signal control circuit includes a transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied and a source connected to a voltage. Bae et al. teaches the use of an NMOS or a PMOS interchangeable to control the driving signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a NMOS instead of a PMOS as the driving signal control circuit, for the purpose changing the activation signal.

4. Claims 33, 36 and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. in view of Park et al.(US 5349559)

With respect to claims 33, 36 and 38, figure 4 of Rhee et al. discloses the circuit above, but fails to disclose wherein the circuit comprises a second switching device. Figure 4 of Park et al teaches the use of a dual transistor CMOS switch to drive a internal control signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art, to use any switch to the driving of the internal voltage driving signal circuit, for the purpose of stability in the switching process.

5. Claims 10-12, 14-17, 23, 25 and 27-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (20020053943) in view of Sher (US 6633196).

With respect to claim 10, figure 1 and 5a of Yamasaki discloses a semiconductor device comprising; a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control

signal (TE), the internal voltage generating circuit comprising a comparing circuit (CMP) for comparing a reference voltage (Vref) to an internal voltage (IntVcc) to generate a comparing signal; a switching circuit (DR) coupled (to connect for consideration together) to both the control signal generating circuit (3) and an output of the comparing circuit (CMP) for receiving the control signal and for transmitting the comparing signal as a driving signal when the control signal (TE) is inactivated; a driving signal control circuit (2) inactivating the driving signal when the control signal is activated; and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal but fails to disclose wherein the switching circuit includes a CMOS transmission gate. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to claim 11, the above circuit produces the circuit of claim 10 wherein the driving signal control circuit includes an NMOS transistor (2f) which has a drain connected to the driving signal generating terminal (via 2ba) for generating the driving signal, a gate to which the control signal (TE) is applied, and a source connected to a ground voltage.

With respect to claim 12, the above circuit produces the circuit of claim 10 wherein the internal voltage driving circuit includes a PMOS transistor (DR) which has a source to which the external power voltage is applied (EX) a gate to which the driving signal is

applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage (IntVcc) wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage when the driving signal is inactivated.

With respect to claim 14, the above circuit produces the circuit of claim 10 but fails to produce the control signal generating circuit wherein the input signal is generated using a fuse. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to one of ordinary skill in the art to use a fuse to generate an input signal for the purpose of making the input signal irreversible.

With respect to claim 15, the recitation of the control signal generating circuit comprising an external pad to generate the control signal responsive to the input signal is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 16, the circuit above produces the circuit of claim 10, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

With respect to claim 23, figure 1 and 5a of Yamasaki discloses a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal

indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control signal (TE) and comparing a reference voltage (Vref) to an internal voltage (IntVcc) to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, wherein the internal voltage generating circuit comprises at least one of a first switching circuit (2e) that cuts off an external power voltage applied to the internal voltage generating circuit when the control signal (TE) is activated, a second switching circuit (2f) that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal (TE) is activated and a third switching circuit (2c) but fails to disclose the third switching circuit including a CMOS transmission gate which transmits the driving signal when the control signal is inactivated. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to 25, the circuit above produces the circuit of claim 23, wherein the internal voltage generating circuit includes a comparing circuit (CMP) for comparing the

reference voltage to the internal voltage (IntVcc) to generate a comparing signal; the third switching circuit (DR) for transmitting the comparing signal as a driving signal when the control signal is control signal is inactivated; a driving signal control circuit (2) for inactivating the driving signal when the control signal is activated and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal.

With respect to claim 27, the above circuit produces the circuit of claim 23 but fails to produce the circuit wherein control generating circuit comprises a fuse to generate the control signal responsive to the input signal. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to one of ordinary skill in the art to use a fuse to generate an input signal (in the control signal generating circuit) for the purpose of making the input signal irreversible.

With respect to claim 28, the recitation of the control signal generating circuit comprises an external pad to generate the control signal responsive to the input signal is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 29, the circuit above produces the circuit of claim 23, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

Response to Arguments

6. Applicant's arguments filed 5/11/2007 have been fully considered but they are not persuasive.

With respect to applicant's argument that this is support in the specification for the limitation of the data bits being simultaneously input to the semiconductor, the Examiner agrees. However the signal PDPDEB is simultaneously input into 58, 42 at the same time as PDPDE is simultaneously put into 60, 68 and 50. Support for this claim is found in column 6, lines 41-50 and states "FIG. 4 is constructed such that in the normal operating mode (e.g., the first operating mode), the PMOS transistors 68,60, having an nput of the control signal PDPDE of "low" through its gates, are turned On. Thus, the supply of the EVC is the operating voltage source of the internal circuit 56, as shown in FIG. 6, (EVC-IVC). At this time, the PMOS transistor 42, 58, having an input of the complementary control signal PDPDEB through its gates, are turned Off and the mode conversion internal voltage source generator 61 is disabled." This would illustrate that the signals PDPDE and PDPDEB are operating at the same time or "simultaneously".

With respect to applicant's argument that the number of bits being greater than one bit is claimed and supported in the specification, the examiner agrees. No new matter has been added, however the added amendments still do not put the case in condition for allowance. At least two bits are put into the semiconductor device because at least one bit is input into 42 and at least one bit is input into 58 to make the semiconductor active. Each bit separately comprises one bit to make the

semiconductor active. Alternatively one low bit is put into 42 and one high bit is put into 50, for a total of two bits activating the semiconductor. Furthermore, during two consecutive bits in the first mode, the circuit still is activated.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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